# Lab 1 Behavioral Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? **Yes**

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: **\_\_\_\_**

Student Name: Wonhee Lee  
Student ID: 54872959  
Date Completed: April 9th, 2020  
Time Spent: Reviewing Digital Design Material: 10 min  
 Design/Preparation Work: 20 min  
 VHDL Coding & Debugging: 1 h

## Behavioral Overview

100%

I first made the truth table of this project and converted it to K-map so that I could make an equation easily. After that, I wrote the code, then changed the testbench to check all outputs by testing all 16 possibilities. After that, I ran a simulation and get a time graph as attached below.

## Lab 1 Truth Table

Provide your truth table for Lab 1 here. You can create a table in Word, Excel, or attach a picture of your truth table as long as it is legible.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Fuel3 | Fuel2 | Fuel1 | Fuel0 | FuelWarningLight |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| F1 F0  F3 F2 | 00 | 01 | 11 | 10 |
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 0 | 0 | 0 | 0 |

## Lab 1 Minimized Equation

F3’F2’ + F3’F1’F0’

## Lab 1 Estimated Delay

List your estimated delay here (you are not required to add the delay to the actual vhdl code for behavioral): 5.2 ns

## Lab 1 Behavioral Simulation Graph

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

